ASSESSMENT OF RELIABILITY OF METAL-OXIDE-SILICON DEVICES

By

Leon Hamiter
Quality and Reliability Assurance Laboratory

and

Ben Bagley
Astrionics Laboratory

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ASTRIONICS LABORATORY

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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George C. Marshall Space Flight Center

SUMMARY

This paper assesses Metal-Oxide-Silicon (MOS) monolithic microcircuit usability and reliability as they affect possible use for certain space applications. Predominant failure modes and mechanisms are identified, failure rates are quantitatively assessed, and quality standards and test programs to reduce failures are recommended. User and manufacturer data presented substantiates a reasonable reliability and indicates MOS device suitability for high reliability use when properly controlled.

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The Metal-Oxide-Silicon (MOS) Monolithic Microcircuit is stimulating intense interest in the electronic industry. This device has the potential to offer many of the same advantages over the conventional diffused bipolar microcircuit that the transistor originally had over the vacuum tube--reduced system size, weight, and power requirements; lower component cost; and improved reliability. For this reason, here is a tremendous desire to use these devices in certain space applications where they can offer great advantages. It is the purpose of this paper to:

Identify predominant failure modes and mechanisms.
Present a quantitative assessment of their reliability (failure rates).
Recommend quality standards and test programs to reduce failures.

There are three types of MOS microcircuits: (1) P-Channel, (2) N-Channel, and (3) Complementary. This paper covers primarily P-Channel devices, since most of the available data is on this type.

The primary problems experienced with P-Channel have been drift and instability caused by ion migration and contamination within the oxide.

The N-Channel has experienced the same oxide problems plus basic P material and N-P junction deficiencies. The prime advantage offered by an N-Channel is the use of positive voltage instead of negative as required by the P-Channel. However, this can be overcome by the application of simple design practices.

The maximum advantages of MOS microcircuits will only be realized through Complementary devices (P and N channel on one substrate). A complementary logic configuration does not demand as tight a tolerance on the electrical parameters of the P-Channel or N-Channel Transistors. Complementary microcircuits will offer the advantages of:

One supply
Microwatt standby power
Large fan out capability
Good noise immunity
Higher speed operation
Negative or positive going logic

MOS microcircuits employ essentially the same materials and processes used in the manufacture of bipolar microcircuits. However, certain operations and techniques are more critical in MOS. Tolerances on masks and mask alignment are much more critical due to the reduced size of the transistors and metal interconnections. MOS microcircuits are subject to many of the same failure modes as bipolar circuits. Failure modes involving device leakage and certain parameter changes are common to both structures, but threshold voltage variations, gate shorts, and most handling features are unique to MOS structures.

These particular failure modes are generally the result of contamination by absorbed films and loss of integrity of the insulating oxide. Figure 1 lists several failure modes and gives the failure mechanisms and primary source of each mode.

Packaging failures are common to the entire semiconductor technology. General contamination, contamination migration during die attach, and gas and leaks in the final package are among the most common packaging failures. After the device has been packaged, it is still subject to failures during handling.

FAILURE MODE	FAILURE MECHANISM	PRIMARY SOURCE
Increased Device Leakage		
Junction Leakage	Inversion Layer formation Aluminum penetration	Contamination
Crossover Leakage	Insulator defects	Contamination
Parameter Changes		
Threshold voltage	Surface states of the underlying silicon	Lack of structural integrity in the insulator
Capacitance variation	Mobile and immobile charge in the gate region	
Material Failure		
Gate rupture	Oxide failure	Contamination
Crossover insulation rupture		Photolithographic
Interconnect Failure		
Malfunction	Contact failure	Contamination
Open	Lead bond failure	Formation of compounds with undesirable qualities
Short	Metal open	photolithographic & deposition

Figure 1. Device Failure Modes, Mechanisms, and Primary Sources

The most significant failure in the MOS transistor is rupture of the input gate insulator by static charge or stray voltages. The static charge developed on a person can be of sufficient voltage and energy to rupture the input gate insulator, rendering the entire device useless. Device voltages are typically in the 10- to 50-volt range and stray voltages of 80 to 120 volts (as can occur on ungrounded soldering irons, etc.) can rupture the input gate oxide. This failure mode can be minimized by observing proper handling precautions. In addition, most MOS manufacturers now incorporate some input protection scheme in the MOS chip. Gate oxide rupture usually takes the form of shorting from gate metal to the underlying diffused region, rather than to the body (see the schematic cross section in figure 2).

As illustrated, the metal gate extends beyond the gate region into the P-regions to insure that the field-effect channel will occur throughout the entire gate region. Otherwise, if the gate metal mask was misaligned such that a PN junction was not covered, the conducting channel in the gate region would terminate before it reached a P-region and the device would not function. The region of gate metal overlap is the weakest part of the present MOS structure.

There are several potential sources of oxide defects in the MOS processing. Depending upon the mask and etch sequence, the gate oxide under the gate metal overlap can contain a boundary between SiO_2 thermally grown on N-type silicon and SiO_2 grown on P-type silicon. The P-region oxide can have varying amounts of dopant, depending upon the process, and a PN junction can have passed under the gate oxide during the diffusion step. Uncontrolled variations of these occurrences can lead to defects in the gate region oxide. The growth rate of an oxide film already in place is different from that of a fresh film; consequently, the interface between the oxides must accommodate the different growth rates. Distribution coefficients for contamination will be different for SiO_2 grown over N- and P-type silicon, and contamination

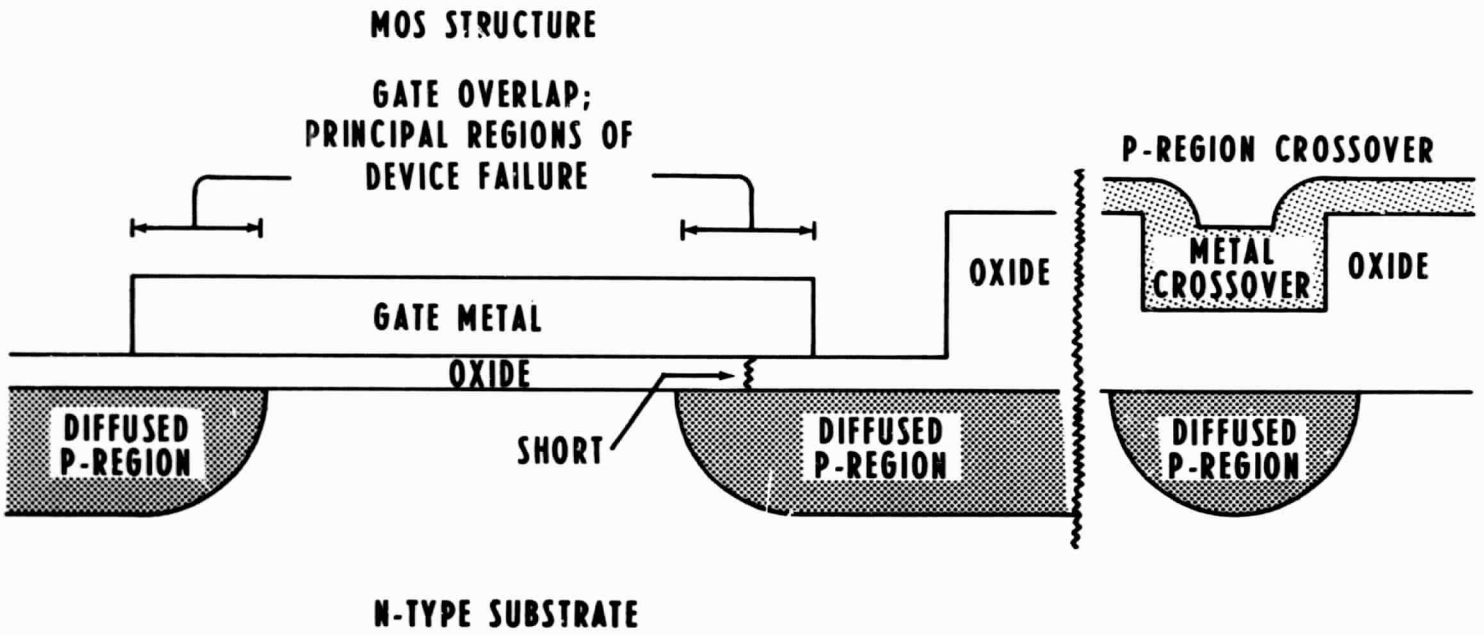

Figure 2. Schematic MOS Structure

concentration in that boundary or at the PN junction beneath the oxide can also lead to structures which cannot survive prolonged stress in an electric field.

Aluminum is the common interconnect metal, and the reaction of aluminum with SiO_2 is known to occur at reasonable rates near 400° to 500°C. Although stress-temperature tests are not conducted in this temperature range, MOS devices are sometimes processed in this range and the reaction could be initiated there. Furthermore, leakage currents through small defects in the oxide can produce local heating which could raise the temperature to where the Al-SiO_2 reaction can proceed at a rapid rate, resulting in rupture of the oxide film. This problem is aggravated by the presence of dopants in the SiO_2.

In order to reduce the threshold voltage, the gate oxide is grown and processed under conditions to minimize the surface charge and to have a minimum useful gate oxide thickness, typically 1000 to 2000 A. Structural and topological defects in the silicon surface, electrical junctions, and contamination in electrical junctions will all contribute to irregularities in the oxide thickness and variations in its insulating properties. Furthermore, the severity of these irregularities can be significantly increased during etching steps.

From the presently available information, it is indicated that oxide failures in MOS devices are the result of defects in the oxide having a spectrum of sizes from a critical size large enough to cause device failure at first test to smaller defects which grow under stress to cause failure after prolonged testing. Further, it is proposed that these defects are the result of electrical, chemical, or physical irregularities in the silicon substrate.

Figure 3 is a graphical comparison by general categories of the failure mechanisms experienced in bipolar and MOS microcircuits. The figures for bipolar are the average by category of three major manufacturers. The

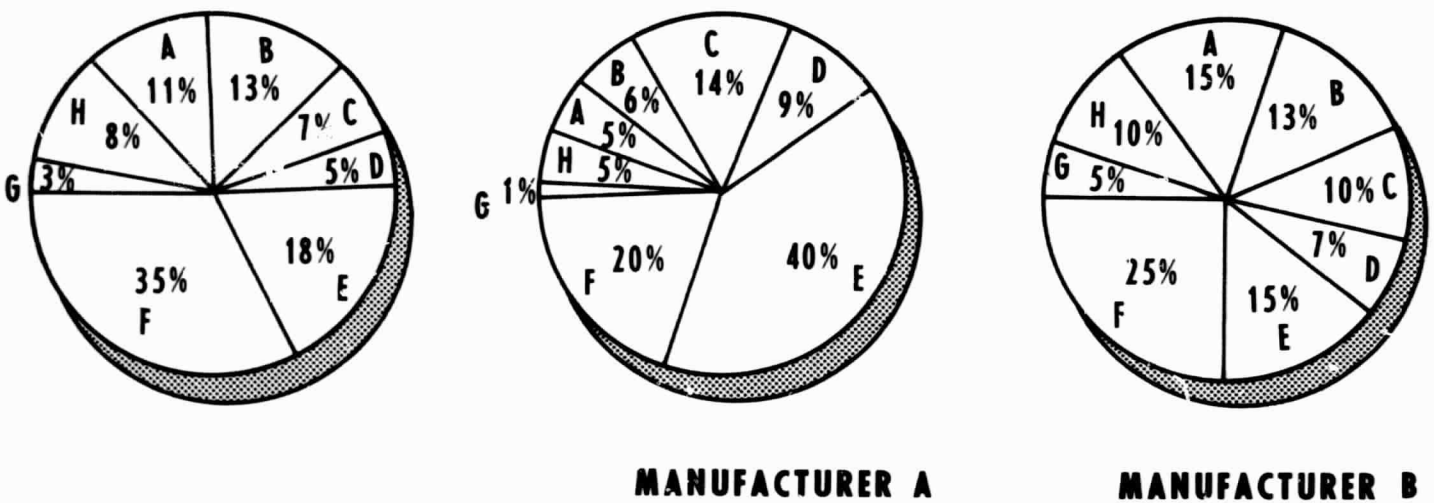

Figure 3. Comparison of Bipolar and MOS Failure Mechanisms

figures for MOS are an average of the two major suppliers. These figures show that the problems at the chip level are about the same for both techniques. The problems with the die mounting and bonding are not significantly different from bipolar. There is some difference in package problems which can be attributed to the more complex MOS microcircuits that are being put in packages with many more leads. The additional leads require more bonds per package, additional area to be sealed with less distance between leads, and smaller cross-sectional area per lead. These conditions tend to make the package more fragile.

The following photographs are examples of the failure mechanisms we have discussed. Figure 4A is a good example of what conducting particles can do to an MOS microcircuit. The spacing between the closest metal stripes is 0.3 mil. The largest burned spot is 2.8 mils long. This photograph illustrates how critical conducting particles can be in microcircuits, especially MOS. In bipolar circuits we have attempted to keep conducting particles to less than 0.5 mil in major dimension. This will not be adequate for MOS where spacing between metallization is 0.3 mil or less. This situation is being controlled with a glass coating of the complete chip.

Figure 4B shows the damage that can result from an overstress static voltage. In this case the rupture occurred at the oxide step and resulted in melting away of gate metal. The gate self-healed twice in this device before the third jolt permanently shorted the gate. The electrical symptom is a 1000 to 2000 ohm linear resistance appearing on the gate lead. This type failure can be prevented by proper handling and zener diode protection.

Figure 4C is an excellent illustration of a static or transient power pulse beyond the handling capability of the protective zener network. This failure showed up as a soft reverse diode breakdown of five to seven volts. This type failure is usually the result of gross mishandling or misapplication.

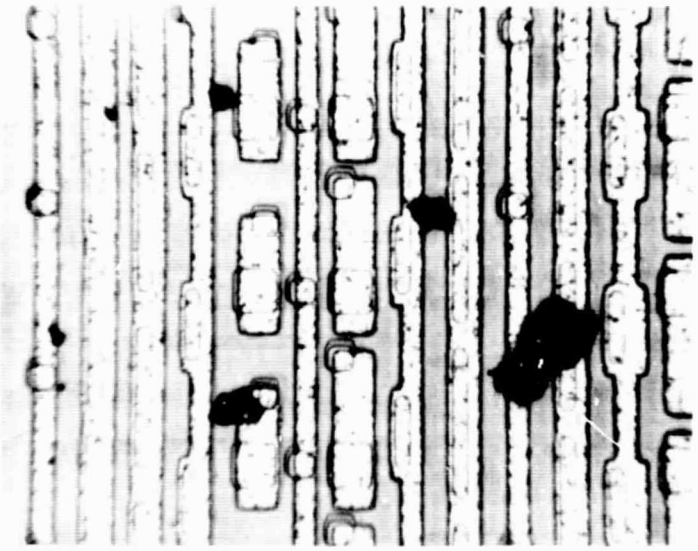

Figure 4A. Results of Conducting Particles

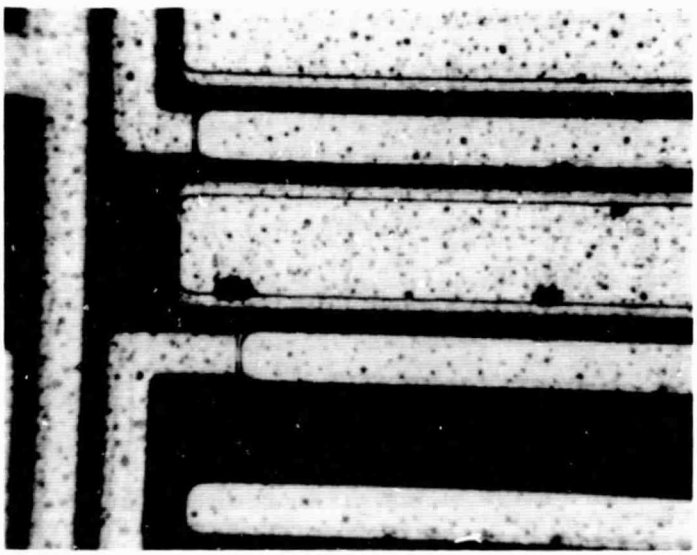

Figure 4B. Rupture of Gate Oxide

Figure 4D shows an improperly mounted die to header. This same problem was encountered with bipolar circuits. It illustrates the need for centrifuge testing as part of screening.

Figure 4E is an example of what occurs when there are partial holes in the oxide and rated voltage is applied. The reduced oxide thickness in the hole area of the P-region is ruptured when exposed to less than rated voltage. Faults such as this can be found with proper electrical testing.

The failure causes observed to date have now been examined. Next a quantitative assessment of data available on MOS Microcircuits is presented in an attempt to quantify how good or bad they are.

Figure 5 contains user data that shows a failure rate which ranges from very high to as low as 0.018 percent/1000 hours. The failure rates for the MSFC tests, in an absolute sense, are not good enough for space applications, bu' it is very limited data and the group of devices represented by this data were built only to prove feasibility. The devices of manufacturer A were also fabricated while the manufacturer was rebuilding the clean room facilities and are not representative of products built under clean room conditions. Also a mistake has been found in the diffusion mask that would cause failure under high temperature stress. The failure of these devices gives an insight for detection of bad devices. The devices tested with no failures represent products built under clean conditions.

The microcircuits represented by the IBM data are from the same manufacturer before modification of the clean room. The available user data is totally insufficient for assessing the device reliability (negative as well as positive) but does indicate the need for tight process controls and inspections. Quality standards must be imposed and enforced at all times.

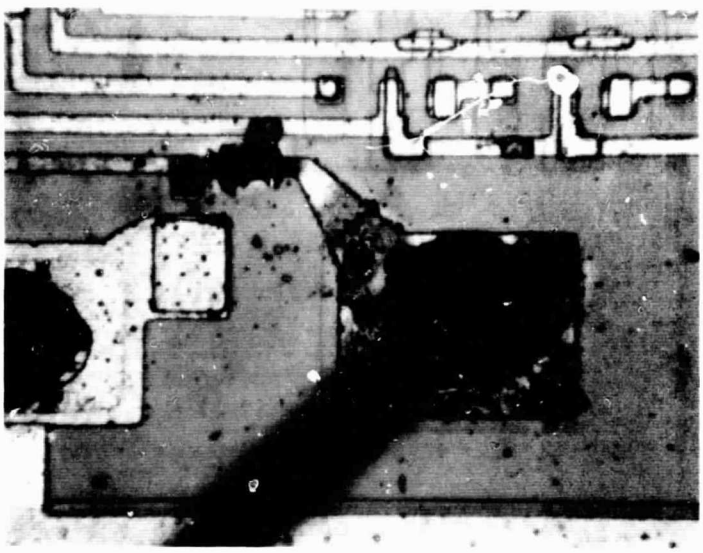

Figure 4C. Damage of Protective Zener Network

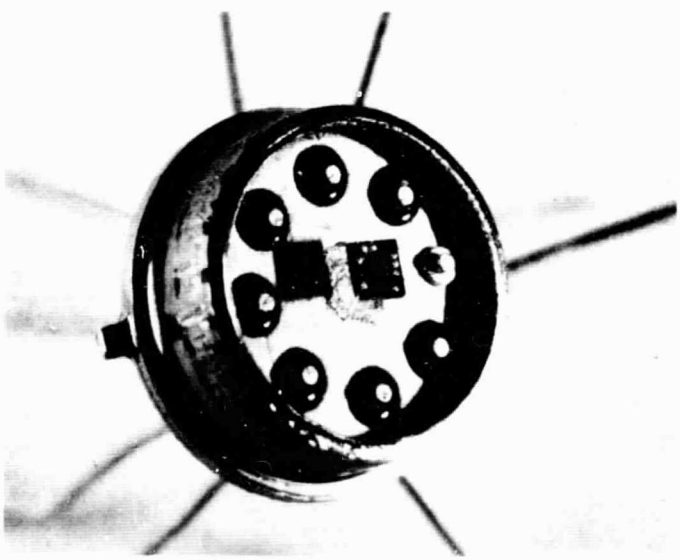

Figure 4D. Improper Die Mounting

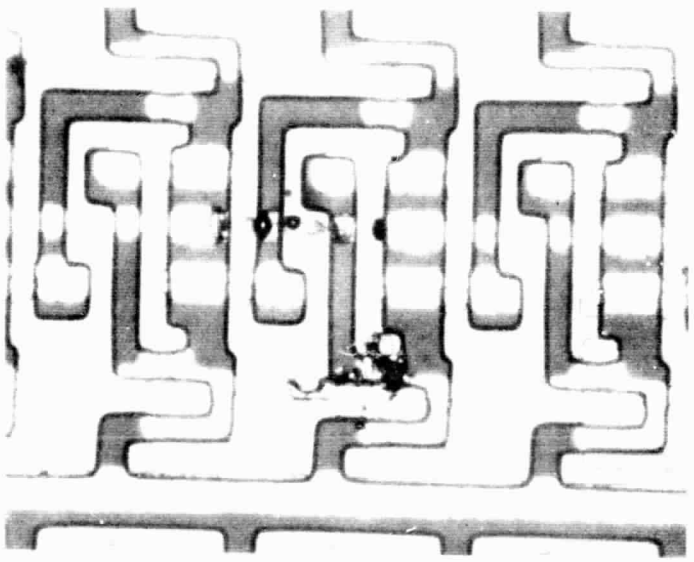

Figure 4E. Damage Due to Pin Holes

USER	CIRCUIT SAMPLES	TEMP.	CIRCUIT HRS	FAILURES	FR/1000 HRS @ 60% CONF
MSFC (MFR A)	5①	25°C - TO 200°C	560.5	5	
MSFC (MFR A)	8②	150°C	1920	0	
MSFC (MFR C)	2③	150°C	624	0	
IBM (MFR A)	16④ 16	25°C 85°C	43,200 43,200	0 0	1.1%
GSFC (MFR B)	2927		17,000,000	2	0.018%

NOTES:

① Units built during clean room modification.

② 4 units before and 4 units after clean room modification

③ Dual complementary flip flops.

④ Digital-Analog converter.

Figure 5. MOS Microcircuit Failure Rates - User Life Test Data

The Goddard Space Flight Center (GSFC) data is from orbital spacecraft operation. These devices were used in three separate spacecraft and the two failures did not occur until after one year of operation.

Figure 6 shows failure rates (FR) calculated from data generated by two manufacturers. Manufacturer A has proven an average microcircuit FR equal to or better than 0.33 percent/1000 hours at 60 percent confidence while manufacturer B has shown 0.038 percent/1000 hours at 60 percent confidence. For comparison and information purposes, MOS microcircuit failure rates have been converted to MOS transistor failure rates and these are shown on the right side of figure 7. The only value of these figures is to show that the failure rates are as good as, if not better than, any experienced with discrete bipolar devices.

For purposes of comparison figures 7A and 7B show failure rates experienced in mid-1966 with bipolar microcircuits by users and manufacturers, respectively. With the proper controls and standards, MOS circuits can equal, if not better, these failure rates today. Figure 8 shows failures encountered during environmental testing. The findings indicate that screening will be necessary for MOS devices as it has been for bipolar.

A comparison of failure rates between bipolar circuits and complex MOS circuits (units which this data represent) does not represent the entire picture. A few complex MOS microcircuits can make a complete component or system which would require many bipolar circuits. Therefore, the failure rates for a few do not have to be as low as the failure rates for many to yield an end item of equal or better reliability.

Figure 9 shows the excellent savings made in total devices for a small serial computer. There is a 60.7 savings factor in total circuits packages plus significant savings in interconnections, crossovers, leads, and areas that

MANUFACTURER	SAMPLES	TEMP.	CIRCUIT HRS	FAILURES	CIRCUIT FR/1000 HRS @ 60% CONF	TRANSISTOR HRS	TRANSISTOR FR/1000 HRS @ 60% CONF
	103	85°C	217,600	0	0.43%	51,380,000	0.0018%
A	40	100°C	40,000	0	2.3%	7,961,000	0.012%
	20	150°C	20,000	0	4.6%	120,000	0.76%
TOTALS	163		277,600	0	0.33%	59,461,000	0.0015%
	408	75°C	3,561,000	0	0.026%	825,284,000	0.00011%
B	552	125°C	1,683,800	1	0.12%	976,270,000	0.00021%
TOTALS	960		5,244,800	1	0.038%	1,801,554,000	0.00012%

Figure 6. MOS Microcircuit Failure Rates - Manufacturers Life Test Data

LEVEL OF TEST	TOTAL DEVICE HRS	FAILURE	FAILURE RATE @ 90% CONF.
SYSTEM	800,000	1	0.48%/1000
SYSTEM	2,000,000	0	0.11%/1000
DEVICE/ SYSTEM	3,408,000	1	0.11%/1000
SYSTEM	1,000,000	2	0.52%/1000
SYSTEM	3,500,000	0	0.063%/1000
COMPUTER	20,000,000	7	0.058%/1000
COMPUTER	6,470,460	0	0.035%/1000
*WEAPONS SYSTEM	N/A	N/A	0.0041%/1000*

*These bipolar microcircuits passed rigid screens and inspections. The failure rate before screening was determined to be 0.348%/1000 hrs.

Figure 7A. Bipolar Microcircuit Failure Rate Data From Users

MANUFACTURER	SAMPLE SIZE	TEMP.	TOTAL DEVICE HRS	FAILURES	FAILURE RATE @ 90% CONF
A	1,683	+55°C	31,649,300	3	0.021%/1000
B	2,013	+125°C	16,059,312	8	0.08%/1000
	4,895	+25°C	46,400,976	0	0.005%/1000
C	1,630	+125°C	4,200,000	3	0.16%/1000 (NOTE 1)
	2,800	+25°C	5,200,000	4	0.13%/1000 (NOTE 2)

NOTE 1. These tests were run under stringent conditions and failure rate will more closely approximate use conditions.

NOTE 2. This data is relatively old and was performed under weak conditions.

Figure 7B. Bipolar Microcircuit Failure Rate Data From Manufacturers

STRESS	SAMPLES	FAILURES
THERMAL SHOCK	6	0
TEMPERATURE CYCLING	6	0
MECHANICAL SHOCK	12	1
CONSTANT ACCELERATION	12	0
VIBRATION	11	1
HIGH TEMPERATURE	10	0
TOTALS	57	2
DEFECTIVE = 3.5%		

Figure 8. Environmental Data

	NO. OF INTEGRATED CIRCUIT PACKAGES	EXTERNAL INTER-CONNECTIONS [a]	INTERNAL INTER-CONNECTIONS [b]	CHIP CROSSOVERS [c]	LEAD BONDS AND WELDS	TOTAL INTER-CONNECTIONS AND CROSSOVERS
BIPOLAR	971	7,736	87,658	137,200	15,472	248,066
MOS	16	176	4,783	18,180	352	23,491
SAVINGS FACTOR	60.7	44	18.3	7.5	44	10.6

a. Integrated circuit package leads or pins.

b. Connections from aluminum to silicon on the chip.

c. Points at which aluminum crosses over P-region above the oxide layer.

Chart shows what is needed to build a small serial computer with conventional monolithic or MOS microcircuits technologies. To fabricate the computer with standard integrated circuits would require 971 units; only 16 integrated circuits are needed if MOS circuits are used. This means that, on the average, one MOS integrated circuit replaces more than 60 conventional integrated circuits. The reduction in interconnections is also impressive, less than 24,000 instead of more than 248,000.

*Courtesy Philco-Ford

Figure 9. Comparison of MOS and Bipolar Circuits in a Small Serial Computer*

decrease reliability. This information was supplied by a manufacturer that builds bipolar and MOS microcircuits, but its accuracy has not been verified.

All this information and data indicates that MOS microcircuits can be obtained and applied in a manner in which they will reliably perform, but quality standards must be established and certain precautions taken.

When the use of a different manufacturer, process, or circuit design is being considered, a series of evaluation or qualification tests should be performed to determine the suitability of the design and device stability.

Once a device has been accepted for an application all products delivered by the manufacturer should be 100 percent screened. Based on the data and information that has been collected and analyzed, the most effective screens and their sequence are as recommended in Figure 10.

The cost of screening of complex MOS microcircuits is approximately the same per circuit as bipolar microcircuits. Because of the reduced quantity of MOS microcircuits required to perform the same functions as bipolar, the net screening cost per end item should be less.

Die inspection - 200X min.

Precap inspection - 40X min.

Temperature cycle - 20 cycles, - 65° to 125°C

Temperature storage - max. rating - 168 hours

Constant acceleration - 20kg - Y1 axis

Hermetic seal (optional)

Electrical tests - +25°C - read & record - critical parameters

High temperature & backbias - max temp - 24 hrs

Electrical tests - +25°C - read & record or go-no go

Burn in - max temp - 240 hrs

Electrical tests

- Read and record critical parameters
- Reject devices which exhibit parameter drift greater than:
    1. Logic levels ±10%
    2. Leakage current
        (a) Low levels +10 times initial
        (b) High levels +20%

Hermetic seal - fine and gross

Radiographic inspection

Figure 10. 100 Percent Screening for MOS Microcircuits

CONCLUSION

- MOS microcircuits offer tremendous power and space reductions. For complementary MOS a power saving factor of 6 is not unlikely and a great increase in complexity per package is possible over bipolar.

- Circuits should be evaluated to assure suitability of design and stability for intended application.

- Circuits should be produced to high quality standards and 100 percent screened to eliminate potential failures.

- The user and manufacturer data substantiates a reasonable reliability and indicates these devices are suitable for high reliability use when properly controlled.

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